

**IN THE CLAIMS**

1. (Previously Presented) An electronic device comprising:  
a substrate; and  
a film disposed above the substrate, the film including:  
LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers; and  
Al<sub>2</sub>O<sub>3</sub> arranged as a layered structure of one or more monolayers.
2. (Previously Presented) The electronic device of claim 1, wherein the film includes La<sub>2</sub>O<sub>3</sub> arranged as a layered structure of one or more monolayers.
3. (Original) The electronic device of claim 1, wherein the film is substantially amorphous.
4. (Original) The electronic device of claim 1, wherein the film exhibits a dielectric constant in the range from about 21 to about 25.
5. (Original) The electronic device of claim 1, wherein the film exhibits an equivalent oxide thickness (t<sub>eq</sub>) in the range from about 1.5 Angstroms to about 5 Angstroms.
6. (Original) The electronic device of claim 1, wherein the film exhibits an equivalent oxide thickness (t<sub>eq</sub>) of less than 3 Angstroms.
7. (Previously Presented) A transistor comprising:  
a body region between first and second source/drain regions in a substrate;  
a film on the body region between the first and second source/drain regions, including:  
LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers; and  
Al<sub>2</sub>O<sub>3</sub> arranged as a layered structure of one or more monolayers; and  
a gate coupled to the film;  
the film being formed by atomic layer deposition including:

pulsing a lanthanum containing precursor into a reaction chamber containing a substrate;

pulsing a first oxygen containing precursor into the reaction chamber;

pulsing an aluminum containing precursor into a reaction chamber; and

pulsing a second oxygen containing precursor into the reaction chamber.

8. (Original) The transistor of claim 7, wherein pulsing a lanthanum containing precursor into a reaction chamber includes pulsing a La(thd)3 (thd = 2,2,6,6- tetramethyl-3,5-heptanedione) source gas into the reaction chamber.

9. (Original) The transistor of claim 7, wherein pulsing an aluminum containing precursor into the reaction chamber includes pulsing a DMEAA source gas into the reaction chamber.

10. (Previously Presented) The transistor of claim 7, wherein pulsing an aluminum containing precursor into the reaction chamber includes pulsing a trimethylaluminum source gas into the reaction chamber.

11. (Previously Presented) The transistor of claim 7, wherein the transistor further includes:  
a floating gate situated between the body region and the gate; and  
a floating gate dielectric disposed on the floating gate, separating the floating gate and the gate, the floating gate dielectric containing LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers.

12. (Previously Presented) A transistor comprising:  
a body region between first and second source/drain regions in a substrate;  
a film on the body region between the first and second source/drain regions, the film including:

LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers; and

Al<sub>2</sub>O<sub>3</sub> arranged as a layered structure of one or more monolayers; and

a gate coupled to the film.

13. (Previously Presented) The transistor of claim 12, wherein the film includes La<sub>2</sub>O<sub>3</sub>.
14. (Previously Presented) The transistor of claim 12, wherein the film is substantially amorphous.
15. (Previously Presented) The transistor of claim 12, wherein the film exhibits a dielectric constant in the range from about 21 to about 25.
16. (Previously Presented) The transistor of claim 12, wherein the film exhibits an equivalent oxide thickness (t<sub>eq</sub>) in the range from about 1.5 Angstroms to about 5 Angstroms.
17. (Previously Presented) The transistor of claim 12, wherein the film exhibits an equivalent oxide thickness (t<sub>eq</sub>) of less than 3 Angstroms.
18. (Original) The transistor of claim 12, wherein the transistor further includes:
  - a floating gate situated between the body region and the gate; and
  - a floating gate dielectric disposed between the floating gate and the gate.
19. (Previously Presented) The transistor of claim 12, wherein the transistor further includes:
  - a floating gate situated between the body region and the gate; and
  - a floating gate dielectric disposed between the floating gate and the gate, the floating gate dielectric containing LaAlO<sub>3</sub>.
20. (Withdrawn) A memory comprising:
  - a number of access transistors, each access transistor including:
    - a body region between first and second source/drain regions in a substrate;
    - a film on the body region between the first and second source/drain regions, the film including:
      - LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers; and
      - Al<sub>2</sub>O<sub>3</sub> arranged as a layered structure of one or more monolayers; and

a gate coupled to the film;  
    a number of word lines coupled to a number of the gates of the number of access transistors;  
    a number of source lines coupled to a number of the first source/drain regions of the number of access transistors; and  
    a number of bit lines coupled to a number of the second source/drain regions of the number of access transistors;  
    the film being formed by atomic layer deposition including:  
        pulsing a lanthanum containing source gas into a reaction chamber containing a substrate;  
        pulsing an aluminum containing source gas into a reaction chamber.

21. (Withdrawn) The memory of claim 20, wherein pulsing a lanthanum containing source gas into a reaction chamber includes pulsing a La(thd)3 (thd = 2,2,6,6- tetramethyl-3,5-heptanedione) source gas into the reaction chamber.

22. (Withdrawn) The memory of claim 20, wherein pulsing an aluminum containing source gas into the reaction chamber includes pulsing a DMEAA source gas into the reaction chamber.

23. (Withdrawn) The memory of claim 20, wherein pulsing an aluminum containing source gas into the reaction chamber includes pulsing a trimethylaluminum source gas into the reaction chamber.

24. (Withdrawn) The memory of claim 20, wherein the memory is a flash memory.

25. (Withdrawn) The memory of claim 20, wherein the memory is a dynamic read access memory.

26. (Withdrawn) A memory comprising:  
    a number of access transistors, each access transistor including:

a body region between first and second source/drain regions in a substrate;  
a film on the body region between the first and second source/drain regions, the  
film including:

LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers; and

Al<sub>2</sub>O<sub>3</sub> arranged as a layered structure of one or more monolayers; and

a gate coupled to the film;

a number of word lines coupled to a number of the gates of the number of access  
transistors;

a number of source lines coupled to a number of the first source/drain regions of the  
number of access transistors; and

a number of bit lines coupled to a number of the second source/drain regions of the  
number of access transistors.

27. (Withdrawn) The memory of claim 26, wherein the film exhibits a dielectric constant in  
the range from about 21 to about 25.

28. (Withdrawn) The memory of claim 26, wherein the film exhibits an equivalent oxide  
thickness ( $t_{eq}$ ) in the range from about 1.5 Angstroms to about 5 Angstroms.

29. (Withdrawn) The memory of claim 26, wherein each access transistor further includes:  
a floating gate situated between the body region and the gate; and  
a floating gate dielectric disposed between the floating gate and the gate, the floating gate  
dielectric containing LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers.

30. (Withdrawn) The memory of claim 26, wherein the memory is a dynamic read access  
memory.

31. (Withdrawn) The memory of claim 26, wherein the memory is a flash memory.

32. (Withdrawn) An information handling device comprising:

a processor;

a memory, the memory including:

    a number of access transistors, each access transistor having:

        first and second source/drain regions in a substrate;

        a body region between the first and second source/drain regions;

    a film on the body region between the first and second source/drain regions, the film including:

        LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers;

        and

        Al<sub>2</sub>O<sub>3</sub> arranged as a layered structure of one or more monolayers;

        and

        a gate coupled to the film;

    a number of word lines coupled to a number of the gates of the number of access transistors;

    a number of source lines coupled to a number of the first source/drain regions of the number of access transistors;

    a number of bit lines coupled to a number of the second source/drain regions of the number of access transistors; and

    a system bus that couples the processor to the memory array;

the film being formed by atomic layer deposition including:

    pulsing a lanthanum containing source gas into a reaction chamber containing the substrate; and

    pulsing an aluminum containing source gas into the reaction chamber.

33. (Withdrawn) The information handling device of claim 32, wherein pulsing a lanthanum containing source gas into a reaction chamber includes pulsing a La(thd)3 (thd = 2,2,6,6-tetramethyl-3,5-heptanedione) source gas into the reaction chamber.

34. (Withdrawn) The information handling device of claim 32, wherein pulsing an aluminum containing source gas into the reaction chamber includes pulsing a DMEAA source

gas into the reaction chamber.

35. (Withdrawn) The information handling device of claim 32, wherein pulsing an aluminum containing source gas into the reaction chamber includes pulsing a trimethylaluminum source gas into the reaction chamber.

36. (Withdrawn) The information handling device of claim of claim 32, wherein each access transistor further includes:

a floating gate situated between the body region and the gate; and  
a floating gate dielectric disposed between the floating gate and the gate.

37. (Withdrawn) The information handling device of claim 32, wherein the information handling device is a computer.

38. (Withdrawn) An information handling device comprising:

a processor;

a memory, the memory including:

a number of access transistors, each access transistor having:

first and second source/drain regions in a substrate;

a body region between the first and second source/drain regions;

a film on the body region between the first and second source/drain regions, the film including:

LaAlO<sub>3</sub> arranged as a layered structure of one or more monolayers;

and

Al<sub>2</sub>O<sub>3</sub> arranged as a layered structure of one or more monolayers;

and

a gate coupled to the film;

a number of word lines coupled to a number of the gates of the number of access transistors;

a number of source lines coupled to a number of the first source/drain regions of

the number of access transistors; and  
a number of bit lines coupled to a number of the second source/drain regions of  
the number of access transistors; and  
a system bus that couples the processor to the memory array.

39. (Withdrawn) The information handling device of claim 38, wherein the film exhibits a dielectric constant in the range from about 9 to about 30.

40. (Withdrawn) The information handling device of claim 38, wherein the film exhibits an equivalent oxide thickness ( $t_{eq}$ ) in the range from about 1.5 Angstroms to about 5 Angstroms.

41. (Withdrawn) The information handling device of claim 38, wherein the memory is a flash memory.

42. (Withdrawn) The information handling device of claim 38, wherein the memory is a dynamic read access memory.

43. (Withdrawn) The information handling device of claim 38, wherein each access transistor further includes:

    a floating gate situated between the body region and the gate; and  
    a floating gate dielectric disposed between the floating gate and the gate, the floating gate dielectric containing LaAlO<sub>3</sub>.

44. (Withdrawn) The information handling device of claim 38, wherein the processor is a microprocessor.

45. (Withdrawn) The information handling device of claim 38, wherein the information handling device is a computer.